**UNIT IV**

**Applications of Counters**

**Binary Decade Counter and decoding gates:**

The binary decade counter is a very useful form of counter. It provides a means of changing a count from less familiar binary code to an equivalent more familiar decimal code.

If the 10 discrete states of decade counter are decoded, the series of waveforms as shown below can be obtained. These waveforms can be used for number of purposes.



**FIG 4.1: Waveform diagram of decoding gates of Up Counter**

One of the most useful methods of utilizing these 10 outputs is to cause them to control 10 lamps which represent 10 decimal numbers. In order to produce 10 waveforms as shown in figure, it is necessary to decode the four flip flops in the counter. Each of 10 states represents a unique condition of four flipflops. For this we require 10, 4 input AND gates.

Count 0 can be recognized as unique time when A, B, C and D are low so that $\overbar{A}$ $\overbar{B}$ $\overbar{C}$ $\overbar{D}$ are all high. Thus, count 0 can be decoded by AND gate with inputs $\overbar{A}$ $\overbar{B}$ $\overbar{C }and$ $\overbar{D}$ are all high. Thus, count 0 can be decoded by AND gate with inputs $\overbar{A}$ $\overbar{B}$ $\overbar{C }and$ $\overbar{D}$. Figure 4.2 shows 10 decoding gates from count 0 to 9.





**FIG 4.2: Decoding gates for counts from 0 to 9**

Figure 4.3 shows one of the methods to build Mod 10 counter. A decade counter can be constructed as shown below. This is Mod-10 counter since it has 10 discrete states. Note that counter proceeds through natural counts up to 10th state i.e. it counts in binary sequence from 0 to 9, i.e. total 10 states.



**FIG 4.3: Circuit diagram of Decade Counter**

In order to skip next state i.e. (1010), $\overbar{D}$ is connected to J input of second flipflop. As $\overbar{D}$ is 0 during 10th count, it will make B flipflop to RESET, since during this count J=0 and K-=1.

Now, as B RESETS, means 0 to 0 transition. So, no change in B forces C to remain in same RESET condition. Now, as no change in B and C makes D flipflop to RESET. Thus, after 10th count, all flipflops will be RESET and it proceeds to count 0. Thus, this is a decade counter. The truth table and waveform diagram are shown in figure 4.4 and Table 4.1 respectively.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| D | C | B | A | CLK |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |

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**FIG 4.4: Waveform diagram of Decade Counter Table 4.1: Truth table of Decade
 Counter**

**BCD Counter 2421**

It is sometimes desirable to construct counter with count sequence other than a straight binary code. We construct modified 2421 BCD counter as shown below.



**FIG 4.5: Circuit diagram of BCD (2421) Counter**

The operation of BCD 2421 counter can be explained as follows.

A must change state each time the clock goes low. Therefore, A changes state at every alternate clock pulses.

B must change state each time A goes low except during the transition from count 7 to count 8. The output of NAND gate is low, whenever C and $\overbar{D}$ are both high. This is true till count 7. As J=1 and K=0, the flipflop B will SET instead of toggle.

Flipflop C is driven by output of B flipflop. Both J and K are high as they are connected directly to Vcc. Flipflop C will toggle each time B goes low.

Flipflop D must change state whenever B and C are high and A goes low. This happens at the transition from count 7 to count 8. Till the 8th pulse, the output of D flipflop is zero.

This is a decade counter and therefore it has only 10 states. There are six illegal/omitted states. They are 1000, 1001, 1010, 1011, 1100 and 1101.

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| --- | --- |
|  |  |

 **FIG 4.6: Waveform diagram of BCD Decade Counter Table 4.2: Truth table of**

 **BCD Decade Counter**

The waveform diagram of BCD 2421 counter is shown in Figure 4.6 and the truth table in Table 4.2 respectively.

**Up/Down Counter:**

The counters discussed till now, counts in the upward sequence as 0, 1,2, …… n-1. It is sometimes useful to count in down sequence. The three flipflop ripple counter is used to count in the upward sequence as 0, 1, 2, 3, ----7. If the flipflops are allowed to trigger from the false side, it will result in a counter that counts in a down sequence i.e. 7 ,6 ,5, ….0.

A 3-bit Up counter and Down counter are shown in Figure 4.7 and 4.8 respectively along with the truth tables for Up and Down counters.



**FIG 4.7: Circuit diagram of 3-bit Up Counter**

A down counter can be formed by triggering the input with the false side of the previous flipflop instead of true side. Such counter is shown in figure 4.8.



**FIG 4.8: Circuit diagram of 3-bit Down Counter**

 Note that exactly same decoding gates are required for count down sequence. It is necessary to change the number labels on the output of each gate. 0→7, 1→6, 2→5, 3→4, 4→3, 5→2, 6→1, and 7→0. The waveform diagram of countdown sequence are shown below.

Notice A changes state each time the clock goes low as before. However, B now changes state when A goes high since this is time when $\overbar{B}$ goes low. In order to unify this data, a three flipflop Up-Down counter is shown in Figure 4.9. In order that counter will progress through a count up sequence, it is necessary to trigger each flipflop with the true side of previous flipflop. If Count UP line is high and Count Down line is low. In order to cause the counter to progress through a count down sequence, it is necessary to hold the Count Up line low and Count Down line high. This causes each flipflop to be triggered from the false side of previous flipflop and cause the counter to progress through countdown sequence.



**FIG 4.9: Circuit diagram of Up/Down Counter**

**3 -BIT SHIFT COUNTER**

Shift counter is used to shift the data in cyclic order. Figure 4.10 shows shift counter using three flipflops. It uses feedback mechanism for shifting data.



**FIG 4.10: Circuit diagram of 3-Bit Shift Counter**

Assume that initially all flipflops are in a RESET condition. Clock is allowed to run. Since $\overbar{C}$ is high and C is low, J=1 and K=0 for A flipflop. Thus, on the negative edge of the pulse, first flipflop will SET. At the same time B and C remains in the RESET condition. Since J=o and K=1 for these flipflops.

During second cycle of clock, A remains high, since $\overbar{C}$ is still high and C is low. At the same time, B will SET as J=1 and K=0. But C remains in RESET condition, since J=0 and K=1 for C flipflop. During the third clock pulse, A and B remains high and C is SET high, since B is now high. Thus, after three cycles of clock, all three flipflops have been changed from low state to high state.

During the fourth clock pulse, $\overbar{C} $is low and C is high and A therefore is RESET to the low state, while B and C remains high. During the fifth cycle of the clock pulse, A remains low, B is RESET, since A is low and $\overbar{A}$ is high and C remains high. During the sixth cycle of the clock pulse, the counter returns to the initial starting point since C is RESET to 0. Thus, this shift register with inverse feedback has progressed through a complete cycle of counts in six clock pulses. The waveform diagram and truth table of 3-bit Shift counter is shown below in figure 4.11 and Table 4.4 respectively.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
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|  |  |  |  |
| --- | --- | --- | --- |
| C | B | A | CLK |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 1 | 1 | 3 |
| 1 | 1 | 0 | 4 |
| 1 | 0 | 0 | 5 |
| 0 | 0 | 0 | 6 |

 |  |

**Table 4.3: Truth table of 3-bit Shift FIG 4.11: Waveform diagram of 3-Bit Shift
 Counter Counter**